REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-29 in the application. In the previous response, the Applicant amended Claims 11, 16 and 21. In the present Examiner's Final Rejection, the Examiner has indicated that Claims 1-10 and 21-29 are allowed and has objected to Claims 3-4 and 23-24. The Applicant believes that the other pending claims are also allowable.

In the present response, the Applicant has amended Claims 3-4 and 23-24 to correct informalities and place the claims in a better condition for appeal. No claims have been canceled or added. Accordingly, Claims 1-29 are currently pending in the application.

I. Rejection of Claims 3-4 and 23-24 under 35 U.S.C. §112

The Examiner has rejected Claims 3-4 and 23-24 under 35 U.S.C. §112, second paragraph for being indefinite and failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. In response, the Applicant has amended Claims 3-4 and 23-24 to particularly point out the subject matter that the Applicant regards as the invention. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §112, second paragraph, rejection and allow issuance of Claims 3-4 and 23-24.

II. Rejection of Claims 11 and 16 under 35 U.S.C. §102

The Examiner has rejected Claims 11 and 16 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. RE 34,206 to Sayer. The Applicants respectfully disagree since Sayer does not teach a jitter control processor with a receiver stage that includes generating a receive time error

signal as a function of a receive clock signal experiencing jitter and a feedback signal as recited in independent Claims 11 and 16.

Sayer is directed to digital data transmission systems and is applicable for timing recovery in subscriber loop interface circuits. (*See* column 1, lines 11-14.) Sayer discloses a U-interface transceiver including a transmitter and a receiver. (*See* column 4, lines 26-27 and Figure 1.) The transceiver includes a timing recovery circuit 124 having a timing estimator 202 that generates a timing estimate z_n and a voltage controlled oscillator 210 that provides a Baud Rate Clock for the transceiver. (*See* column 5, lines 5-8 and Figures 1-3.) The Examiner asserts the timing estimator 202 discloses generating a receive time error signal as recited in independent Claims 11 and 16. (*See* Examiner's Final Rejection, page 3.)

The timing estimator 202 in Sayer, however, uses an equalized version x_n of a far-end signal, a recovered far-end signal a_n and the Baud Rate Clock to generate the timing estimate z_n. (*See* column 6, lines 47-65 and Figures 1-3.) Neither of these is a receive clock signal experiencing jitter as recited in Claims 11 and 16. More specifically, the equalized far-end signal x_n and the recovered far-end signal a_n are data symbols and the Baud Rate Clock is a recovered baud rate clock signal. (*See* column 7, line 55 to column 8, line 11 and Figures 1-3.) The timing estimator 202, therefore, does not teach generating a receive time error signal as a function of a receive clock signal experiencing jitter as recited in independent Claims 11 and 16. Additionally, the Applicants do not find any other teachings in Sayer that discloses generating a receive time error signal as presently claimed.

Since Sayer does not disclose each and every element of independent Claims 11 and 16, Sayer does not anticipate Claims 11 and 15. Accordingly, the Applicant respectfully requests the

Examiner to withdraw the §102 rejection with respect to Claims 11 and 16 and allow issuance thereof.

III. Rejection of Claims 12-15 and 17-20 under 35 U.S.C. §103

The Examiner has rejected Claims 12-15 and 17-20 under 35 U.S.C. §103(a) as being unpatentable over Sayer. The Applicant respectfully disagrees.

As discussed above, Sayer does not teach generating a receive time error signal as a function of a receive clock signal experiencing jitter as recited in independent Claims 11 and 16. Sayer also does not suggest generating a receive time error signal as a function of a receive clock signal experiencing jitter since Sayer teaches generating a timing estimate based on equalized and recovered data symbols. Sayer, therefore, does not teach or suggest each and every element of independent Claims 11 and 16. As such, Sayer does not provide a *prima facie* case of obviousness of Claims 11 and 16 and Claims 12-15 and 17-20 that depend thereon, respectively. Thus, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 12-15 and 17-20 and allow issuance thereof.

IV. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-29.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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